(12) UK Patent Application (19) GB (11) 2 326 036 (13) A

(43) Date of A Publication 09.12.1998

(21) Application No 9711747.7

(22) Date of Filing 07.06.1997

(71) Applicant(s)
Motorola Limited
(Incorporated in the United Kingdom)
Jays Close, Viables Industrial Estate, BASINGSTOKE, Hampshire, RG22 4PD, United Kingdom

(72) Inventor(s)
Peter Miller

(74) Agent and/or Address for Service
Motorola Limited
European Intellectual Property Operation, Midpoint, Alencon Link, BASINGSTOKE, Hampshire, RG21 7PL, United Kingdom

(51) INT CL^6
G06F 1/04 , H03K 7/08 , H04B 15/04

(52) UK CL (Edition P)
H3A AE AL2DX
G4A AFT
H3P PHX
H3R RL26G1B RPMA
H3T T2C T2F1 T2F5 T2T3F T3N T4D
U1S S2092 S2125

(56) Documents Cited
EP 0163313 A2 DE 002815895 A1

(58) Field of Search
UK CL (Edition O) G4A AFT , H3A AE , H3P PDN PHX , H3R RPMA
INT CL^6 G06F 1/04 1/08 , H03K 7/08 , H04B 15/00 15/04
Online: WPI,INSPEC,JAPIO

(54) Abstract Title
A pulse-width-modulated clock generator producing reduced EMI

(57) The mark-space ratio of a clock signal is modulated 100 by a ramp 120, staircase, or noise waveform so that harmonics associated with clock switching transients are spread out and the maximum harmonic amplitude is reduced. The clock frequency may be locked by a phase-locked-loop 130,140,160,165 to a multiple of the frequency of a crystal oscillator 145,147. Alternatively, the output of a crystal oscillator may be pulse-width-modulated using an inverter or a CMOS gate (figure 1). The circuit may be used in microprocessor systems.

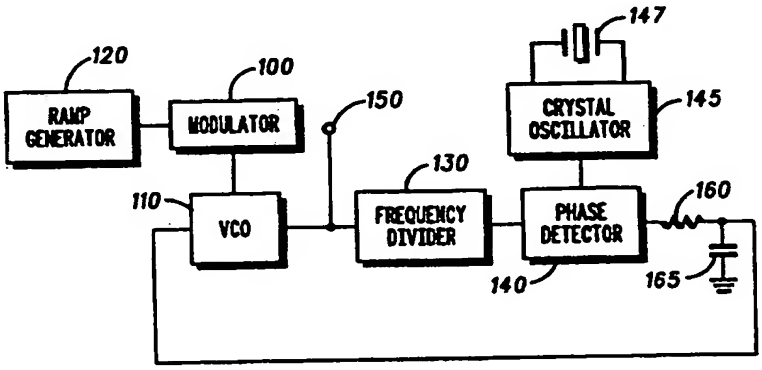

FIG.2

GB 2 326 036 A

At least on drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

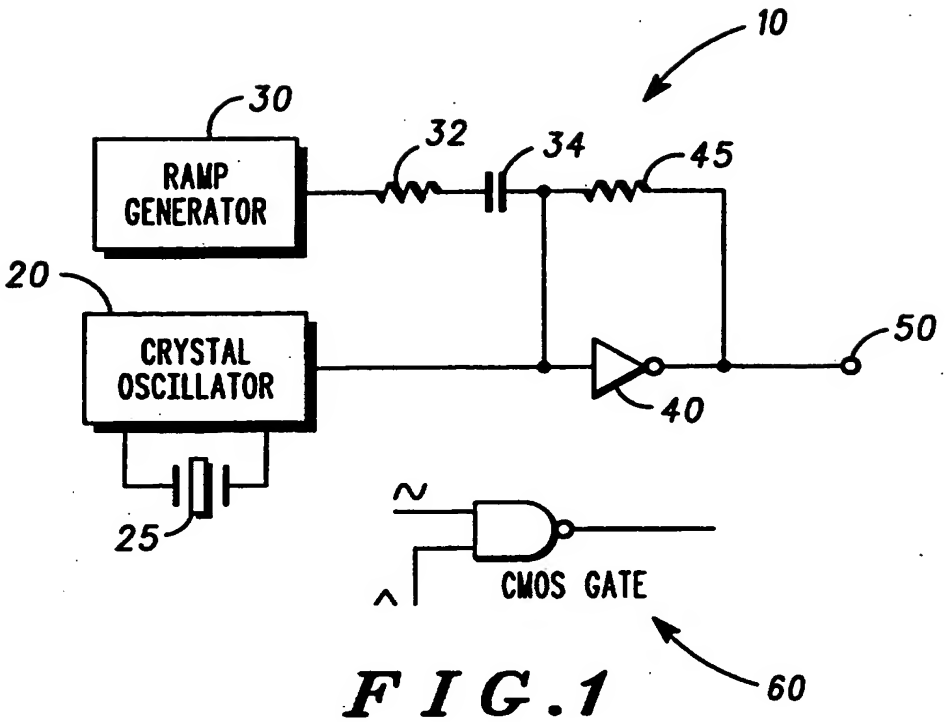
10
30
RAMP GENERATOR
32
34
45
20
CRYSTAL OSCILLATOR
50
40
25
CMOS GATE
60

FIG. 1

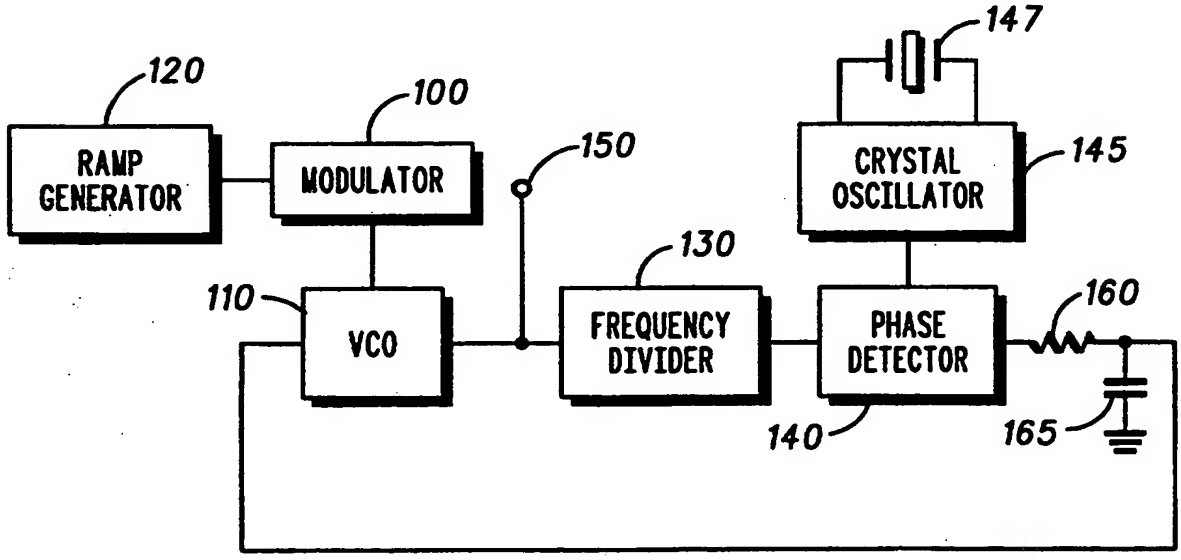
147
120
100
150
RAMP GENERATOR
MODULATOR
CRYSTAL OSCILLATOR
145
130
110
160
VCO
FREQUENCY DIVIDER
PHASE DETECTOR
140
165

FIG. 2

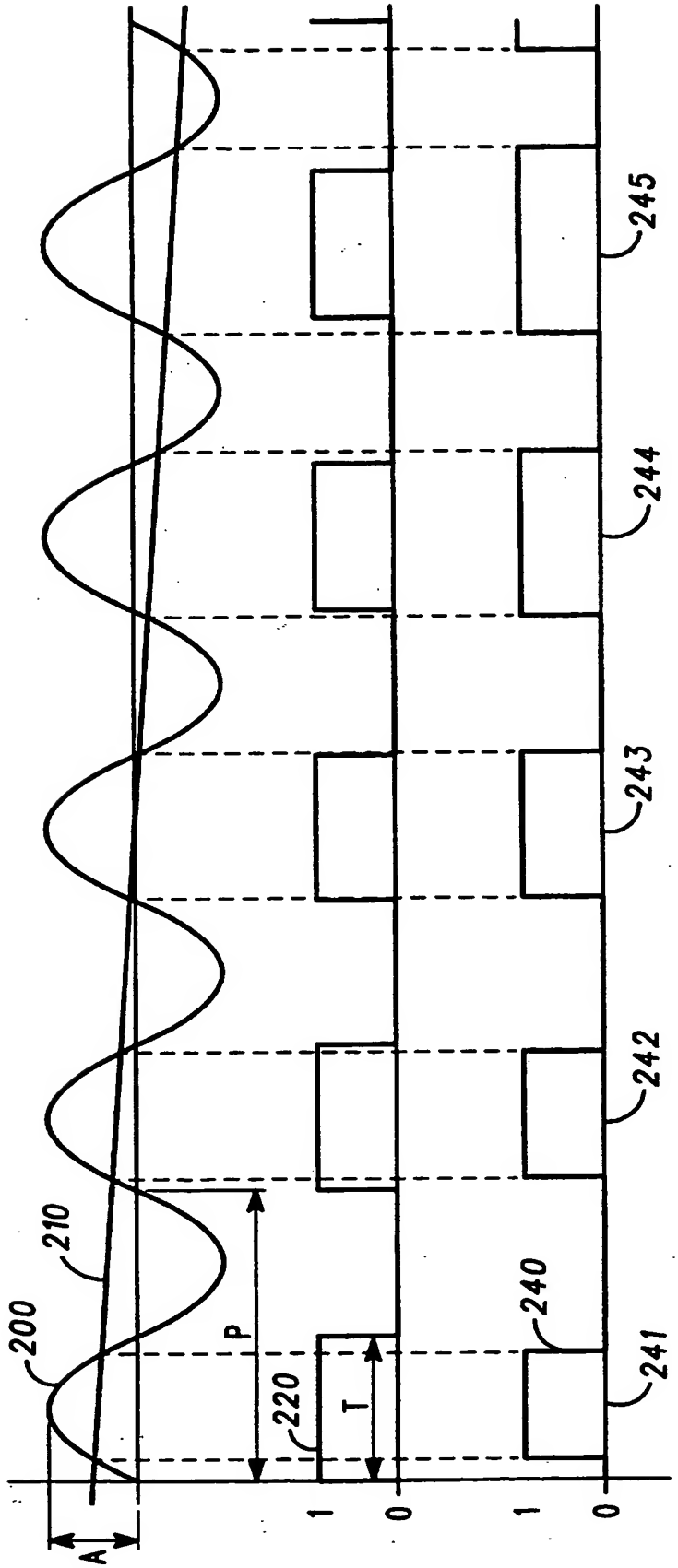

FIG. 3

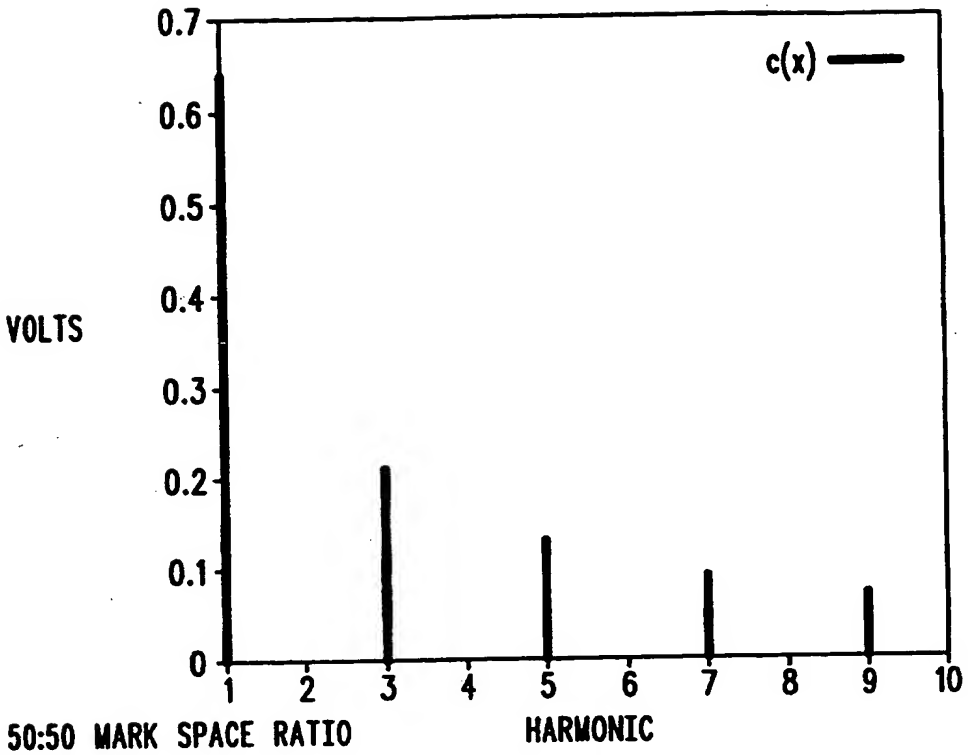
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
c(x)
VOLTS
1
2
3
4
5
6
7
8
9
10
50:50 MARK SPACE RATIO
HARMONIC

FIG.4

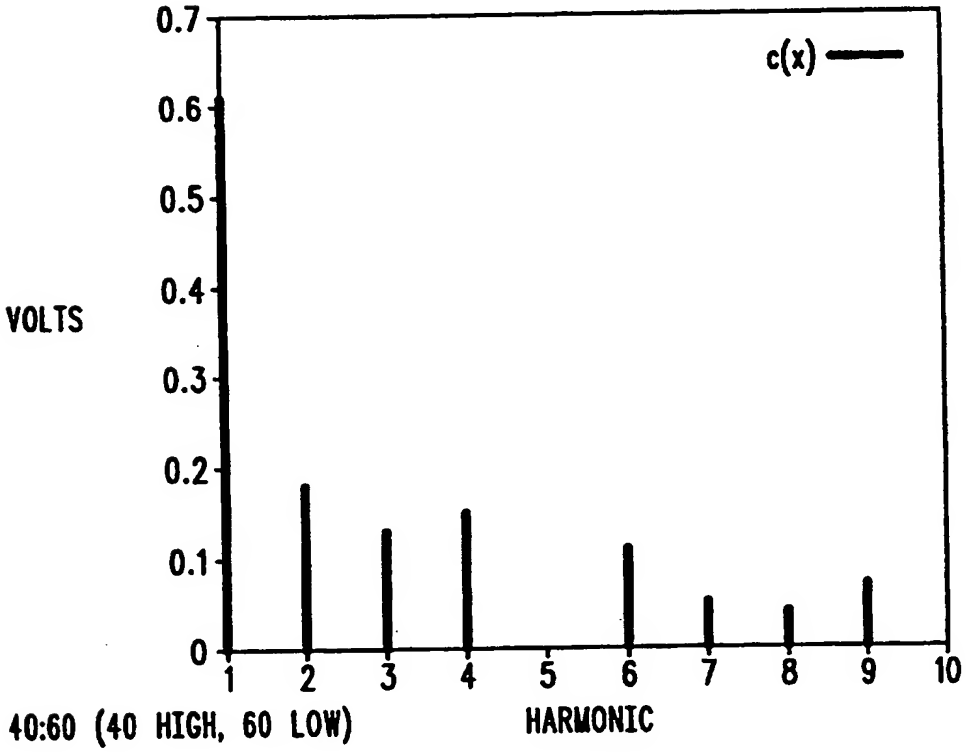
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
c(x)
VOLTS
1
2
3
4
5
6
7
8
9
10
40:60 (40 HIGH, 60 LOW)
HARMONIC

FIG.5

CLOCK CIRCUIT AND METHOD FOR PRODUCING A CLOCK SIGNAL

Field of the Invention

This invention relates to clock circuits, and particularly but not exclusively to clock circuits for use with microprocessors.

Background of the Invention

Every element in a circuit causes electromagnetic emissions due to changes in voltages and currents. In the case of a digital circuit, electromagnetic emissions are associated with a switch of state (high-to-low and low-to-high signal transitions). These emissions can interfere with other pieces of equipment, and legislation in many countries now regulates the maximum permitted level of emissions for any piece of equipment. On 1st January 1996 the European Commission (EC) directive on radiated emissions came into effect. Products which do not comply with the directive cannot be sold in Europe.

In a microprocessor clock circuit, a regularly switched output signal is produced. The clock signal is typically used to synchronise a large amount of circuitry. Therefore emissions associated with a microprocessor clock can be a significant problem.

A known method of reducing electromagnetic emissions in a microprocessor clock involves varying the frequency of the master oscillator by a small amount either side of the required frequency so that the energy emitted at given harmonic frequencies (when time averaged) is reduced.

However, a problem with this arrangement is that that by varying the frequency, timing information derived from the clock signal will also vary. Furthermor all devices have a maximum rated frequency, and for

optimum performance the operating clock frequ ncy should be as close to this as possible. In the case of varying frequ ncy, the upper limit of the frequency variation must be below the allowed maximum, and so the average frequency will be even less. Therefore the average "throughput" of the device will be correspondingly reduced.

This invention seeks to provide a clock circuit and method for producing a clock signal which mitigates the above mentioned disadvantages.

Summary of the Invention

According to a first aspect of the present invention there is provided a clock circuit for providing a pulsed signal, comprising: an oscillator for generating a pulsed signal having a mark-to-space ratio; a generator for generating a varying signal; and, modulation means for modulating the pulsed signal by the varying signal; wherein the mark-to-space ratio of the modulated pulsed signal varies in dependence upon the varying signal, such that harmonic emissions associated with the modulated pulsed signal are substantially ameliorated.

According to a second aspect of the present invention there is provided a method of providing a clock signal to a device, comprising: generating a pulsed signal having a mark-to-space ratio; generating a varying signal; and, modulating the pulsed signal by the varying signal; wherein the mark-to-space ratio of the modulated pulsed signal varies in dependence upon the varying signal, such that harmonic emissions associated with the modulated pulsed signal are substantially ameliorated.

In this way the mark to space ratio of the clock signal is varied over time. This has the effect of changing the amplitude of each of the harmonics - effectively modulating the amplitude of any given harmonic over time.

Therefore the average energy peaks in the harmonic spectrum will be reduced, so reducing the apparent radiation.

Brief Description of the Drawing(s)

An exemplary embodiment of the invention will now be described with reference to the drawing in which:

FIG.1 shows a preferred embodiment of a clock circuit in accordance with the invention.

FIG.2 shows an alternative embodiment of a clock circuit in accordance with the invention.

FIG.3 shows a timing diagram of signals associated with the clock circuit of FIG.1.

FIGs. 4 and 5 show graphs of electromagnetic interference generated at harmonic frequencies associated with a signal of the clock circuit of FIG.1

Detailed Description of a Preferred Embodiment

Referring to FIG.1, there is shown a clock circuit 10, comprising an oscillator 20, a ramp generator 30 and an inverter 40.

The crystal oscillator 20 is coupled to a crystal 25 which, when powered by the oscillator 20, oscillates at a predetermined frequency. The inverter 40 is coupled to receive an oscillating (pulsed) output from the crystal oscillator 20, and is further coupled to provide a clock output signal to the output terminal 50, the clock output signal to be further described below. A

feedback resistor 45 is coupled between the output and the input of the inverter 40.

The ramp generator 30 is coupled via a resistor 32 and a capacitor 34 to the input of the inverter 40, for providing thereat a ramp voltage output to be further described below.

As an alternative to the inverter 40 and resistor 45, a standard CMOS gat 60 could be used, with one input receiving the ramp signal and one input receiving the oscillating output.

Referring now also to FIG.2, there is shown an alternative arrangement for producing a clock output signal, namely a Phase Locked Loop (PLL) circuit. The PLL circuit comprises a voltage controlled oscillator (VCO) 110, a ramp generator 120, a modulator 100, a voltage divider 130 and a phase detector 140. The ramp generator is coupled to provide a ramp voltage to the modulator 100. The VCO 110 is coupled to the modulator 100, and is arranged to oscillate in dependence upon a feedback voltage to be further described below, the oscillation of the VCO 110 also being modulated by the modulator 100. The VCO 110 is coupled to provide a clock signal output to an output terminal 150.

A frequency divider (divide by N) 130 is also coupled to receive the clock signal output from the VCO 110, for providing a divided signal to the phase detector 140. The phase detector 140 is coupled to a crystal oscillator 145, arranged to oscillate a crystal 147 at a predetermined frequency. The phas detector 140 is further coupled to provide an output signal, which is fed back to the input of the VCO 110 via a filter network which comprises, in the simplest implementation, a resistor 160 and a capacitor 165. The basic effect of the PLL circuit is f r the frequency of the signal produced at the output terminal 150 to be N times the frequency of the crystal oscillator 145.

The modulator 100 modulates the VCO 110 such that the mark-space rati of the output signal varies.

In operation, and referring now also to FIG. 3, there is shown a diagram of periodic signals associated with the above embodiments. A sinusoidal signal 200 has amplitude A and time period P, which represents the oscillation of the crystal 25 or 147. A first rectangular wave 220 also has amplitude A, an 'on' time T (which is P/2, or 50% of P) and repetition rate t_r. The mark-space ratio of the first rectangular wave 220 is 50:50, since the 'on' time T is equal to the 'off' time.

The amplitude of the j^{th} harmonic A_j of the rectangular wave can be shown to be:

$$A_j=2AT/t_r ((\sin Tj/T_r)/(Tj/T_r))$$

This gives a spectrum with a main lobe at frequency $Fc=1/t_r$ and zeros at 1/T, 2/T etc.

A ramp signal 210, such as is generated by the ramp generator 30 of FIG.1 or ramp generator 120 of FIG.2, is used to modulate the clock signal provided by the inverter 40 or VCO 110. This is shown schematically by the ramp 210 of FIG.3, which is superimposed on the sinusoidal signal 200.

This has the effect of varying the mark-space ratio of the rectangular wave over time, such that it is constantly changing. The second rectangular wave 240 demonstrates this. The edges of the second rectangular wave 240 occur at the points where the ramp signal 210 crosses the sinusoidal signal 200. The duration of the first and second rectangles 241 and 242 are less than T. The duration of the third rectangle 243 is substantially equal to T (50:50 mark-space ratio), and the duration of the fourth and fifth rectangles are greater than T. In this way the mark-space ratio f the second rectangular wave 240 varies over time.

Referring now also to FIG.4, there is shown a graph of harmonics generated by a 50:50 mark-space rati rectangular wave, such as the first rectangular wave 220, at which only odd harmonics are present.

Small movements away from a 50:50 mark-space ratio change the harmonics and their levels. Referring now also to FIG.5, there is shown a graph of harmonics generated by a 40:60 mark-space ratio square wave. As can be seen from a comparison of the graphs, the levels of the highest amplitude harmonics, the third and fifth, are significantly reduced.

By providing a constantly varying ramp signal such that the mark-space ratio of the clock signal varies between 40:60 and 60:40, the amplitude of each of the harmonics varies over time, such that the average energy peaks associated with the harmonic spectrum of a clock having a 50:50 mark-space ratio are reduced, so reducing the apparent radiation at these peaks.

It will be appreciated that alternative embodiments to the one described above are possible. For example, the modulator 100 could be arranged to modulate the clock signal such that the low-high transition (the leading edge) remains fixed and only the high-low transition (the trailing edge) is moved. In this way the frequency of the leading edge remains constant. Therefore for a circuit having a leading edge triggered clock, there is no frequency variation associated with the mark-space ratio modulation. Similarly, the trailing edge could be fixed and the leading edge could be moved.

As an alternative to the constantly changing ramp signal, it is envisaged that other signals such as a noise signal or a stepped signal could be provided as a varying signal.

Claims

1. A clock circuit for providing a pulsed signal, comprising:
an oscillator for generating a pulsed signal having a mark-to-space ratio;
a generator for generating a varying signal; and,
modulation means for modulating the pulsed signal by the varying signal;
wherein the mark-to-space ratio of the modulated pulsed signal varies in dependence upon the varying signal, such that harmonic emissions associated with the modulated pulsed signal are substantially ameliorated.

2. The clock circuit of claim 1 wherein the clock circuit is a phase locked loop arrangement, the oscillator being a voltage controlled oscillator.

3. The clock circuit of claim 1 wherein the modulation means is an inverter with a feedback resistor.

4. The clock circuit of claim 1 wherein the modulation means is a CMOS gate.

5. A method of providing a clock signal to a device, comprising:
generating a pulsed signal having a mark-to-space ratio;
generating a varying signal; and,
modulating the pulsed signal by the varying signal;
wherein the mark-to-space ratio of the modulated pulsed signal varies in dependence upon the varying signal, such that harmonic emissions associated with the modulated pulsed signal are substantially ameliorated.

6. The clock circuit or method of any preceding claim wherein the varying signal is a constantly varying ramp signal.

7. The clock circuit or method of any one of claims 1 to 5 inclusive wherein the varying signal is a stepwise varying ramp signal.

8. The clock circuit or method of any one of claims 1 to 5 inclusive wherein the varying signal is a noise signal.

9. The clock circuit or method of any preceding claim wherein the frequency of one of the edges of the modulated pulse signal remains substantially constant.

10. A clock circuit substantially as hereinbefore described with reference to the accompanying drawings, and as illustrated by FIG.1 or FIG.2 of the drawings.

11. A method for producing a clock signal substantially as hereinbefore described with reference to the accompanying drawings.

The Patent Office

9

Application N : GB 9711747.7
Claims searched: 1-11

Examiner: K. Sylvan
Date of search: 13 August 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H3P (PDN,PHX), H3A (AE), H3R (RPMA), G4A (AFT)

Int Cl (Ed.6): H04B (15/00,15/04), G06F (1/04,1/08), H03K (7/08)

Other: Online: WPI,INSPEC,JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP0163313 A2	Tektronix. See figure 1A, page 5 lines 7-11, and page 7 lines 25-31.	1,5,6,8,9
X	DE002815895 A1	Rohde & Schwarz. See page 4 lines 21-28 or WPI abstract 79-K2422B/44	1,5,8

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.